HIGH EFFICIENCY POWER HFETS FOR LOW POWER WIRELESS APPLICATIONS

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ABSTRACT

This paper discusses the development of depletion mode Heterojunction FETs (HFETs) for high efficiency power amplifiers. At 850 MHz, a 12 mm HFET achieved power added efficiency of 72 % and an output power of +31.5 dBm at V_{ds} = 3.0V. An optimized HFET achieved 73% pwer added efficiency and 30 dBm output power at V_{ds} = 2.0V. These devices also exhibited a 12 dB improvement in out-of-band noise performance compared to ion implanted MESFETs.

INTRODUCTION

Next generation portable communication products will require devices and circuits that operate at drain biases of ²3.0V. Semiconductor devices with higher efficiencies and better noise figure and gain performance will be required to maintain the same RF performance at lower voltages. The power performance of GaAs HFET devices has been reported (1-2). This paper reports on the device structure, wafer processing, and the DC and RF performance of heterojunction power FETs developed for high efficiency power amplifiers operating at low drain voltages (² 3.0 V).

DEVICE & PROCESSING

A cross section of an HFET structure is shown in Fig 1. The HFET structures were

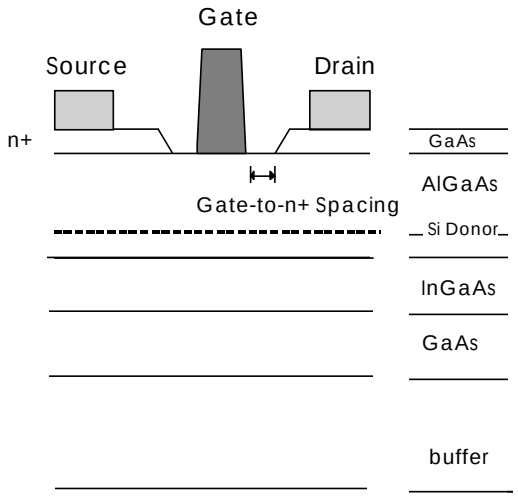

Fig. 1. Cross sectional view of the HFET structure.

grown by MBE on a semi-insulating GaAs substrate. First a superlattice buffer layer was

grown to reduce the defects propagating from the substrate. A thick strained layer of $In_{0.15}Ga_{0.85}As$ channel was grown on the buffer followed by $Al_{0.24}Ga_{0.76}As$. A thick n^+ cap layer was then grown to provide good ohmic contacts to the channel. Planar doping was used in these structures to increase the efficiency of the carrier transfer from the large bandgap AlGaAs supply layer to the InGaAs. Planar doping also results in a separation between the gate metal and the donor layer by an undoped AlGaAs layer. This decreases the electric field around the edges of the gate metal and consequently increases the breakdown voltage.

The power HFETs were fabricated using a standard process for microwave devices. This consists of Au/Ge/Ni ohmic contacts, Ti/Al gate, Si_3N_4 passivation and Ti/Au interconnect metal. The on-resistance and the gate-drain breakdown voltage were the two critical parameters that were optimized for the low voltage operation of these devices. Since the spacing between the n^+ GaAs cap layer and the edge of the gate metal effects both the on-resistance and the breakdown voltage of the device, this spacing was optimized through design of experiments.

RESULTS

DC and RF characteristics of an HFET with a 1.2 µm gate length and 12 mm gate width were measured. The devices exhibited a 3.0A saturation current with on-resistance of about 0.2 ½. The gate-drain breakdown voltage was greater than 12V.

Power measurements such as output power, gain and power added efficiency (PAE) were measured using an automated load-pull system. Fig. 2 shows the measured performance of a typical device at 850 MHz. The HFET device achieved a power added efficiency of 72 % at an output power level of +31.5 dBm with a corresponding power gain of 11.5 dB at V_{ds}=3.0V.

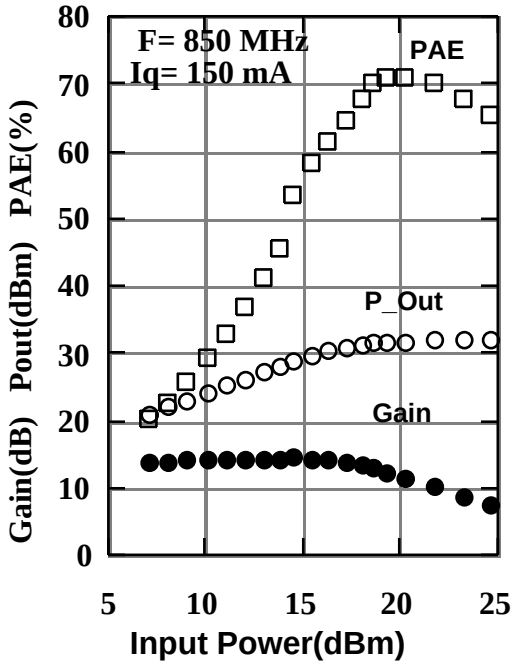

Fig. 2 Swept power measurement of an HFET at 3V. (Gate Width=12 mm)

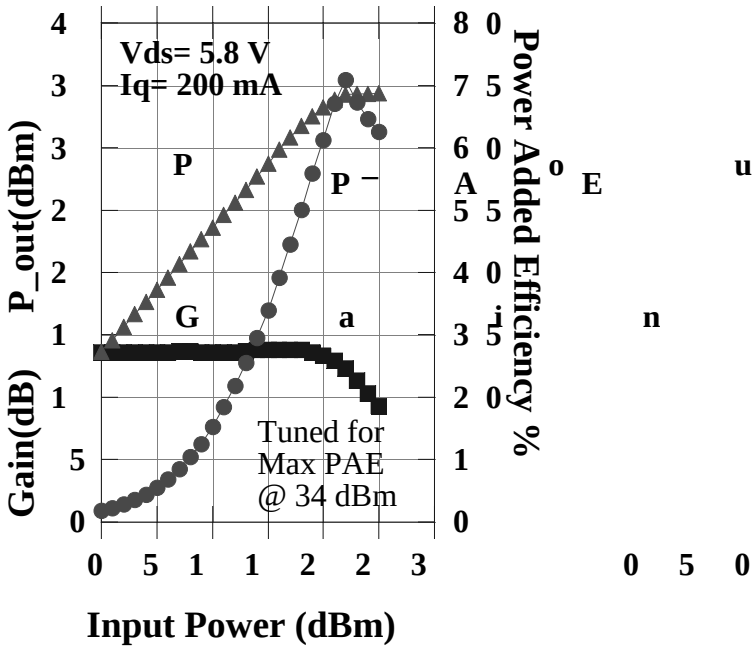

Fig 3. Measured Power Output, PAE and Gain of HFET @ 5.8 V(Gate Width=12 mm)

In Fig. 3, the performance of the same power HFET at Vds=5.8V is shown. The device was tuned for maximum power added efficiency at an input power of 20 dBm and a quiescent drain to source current of 200 mA. The plot shows gain, output power and PAE versus input power. A maximum power added efficiency of 70 % and power gain of 12 dB were achieved at an output power of 34 dBm.

In Fig. 4, the performance of the device as a function of drain bias is shown. In this case, source and load impedances were presented to the device which produced a reasonable trade-off between power output and efficiency at Vds=3.0V. Measurements at other bias points were performed without further tuning. This device has impressive performance at lower drain voltages as well. At Vds=2.0V, a 65% power added efficiency and +28.5 dBm output power were achieved.

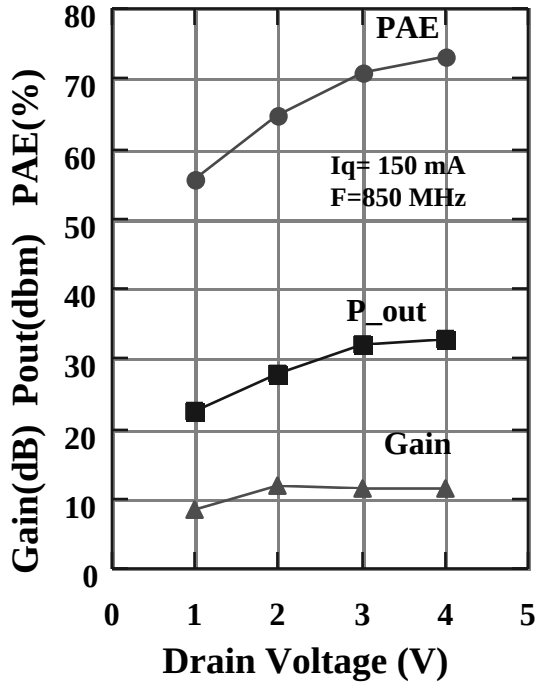

Fig. 4. The Pout, Efficiency and gain as function of Vds (Device Width= 12 mm)

Fig. 5 shows the measured performance of a 27 mm power HFET at V_{ds}=2.0V. The device achieved a power added efficiency of

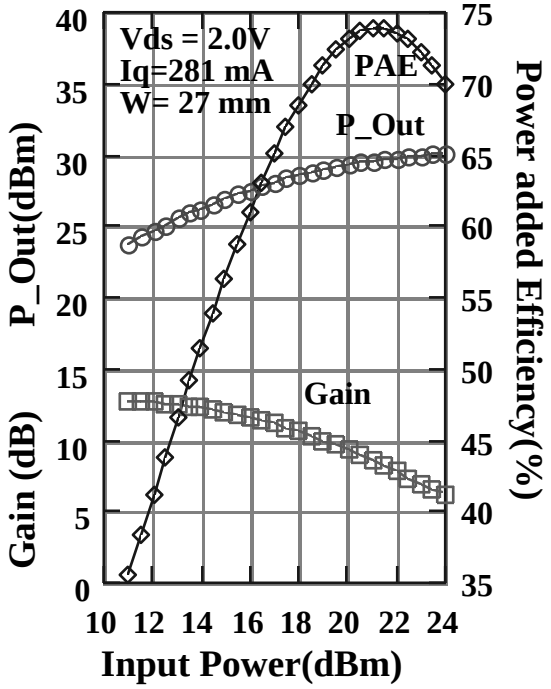

Fig. 5. Measured Gain, Power Output and PAE of HFET @ 2.0 V.

73% at an output power of 30 dBm. To the best of our knowledge, this is the highest power added efficiency reported to date for this output power level at Vds=2.0V.

These power HFETs were further characterized for their out-of-band noise performance. In full-duplex systems, out-of-band noise is the noise generated at receive band frequencies by power amplifiers operating in the transmit band. Since the transmit and receive channels are only 45 MHz apart, this noise can desensitize the receiver performance. A power amplifier that exhibits lower out-of-band noise characteristics allows the relaxation of the duplexer specifications. A hybrid amplifier was designed using the power HFETs and the out-of-band noise properties were measured at

the cellular frequency band. Fig. 6 shows the out-of-band noise performance for a 12 mm HFET operating at a drain to source voltage of 3.5V. The noise power at the output of the hybrid amplifier was measured as dBm in a 30 kHz bandwidth. The device exhibited an out-of-band noise performance of -112dBm/30kHz bandwidth. An ion implanted MESFET exhibited only -100dBm/30kHz when measured in the same configuration.

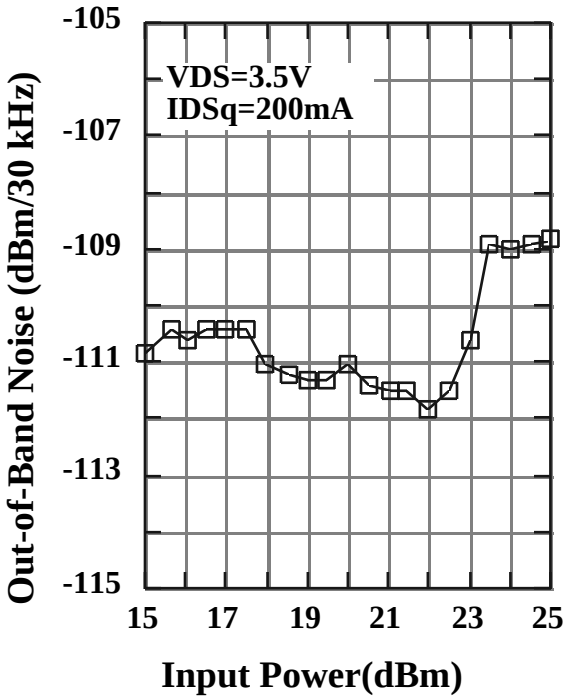

Fig. 6. Measured o ut-of-band noise of a 12 mm HFET

CONCLUSIONS

A high efficiency power HFET device was designed, fabricated and tested for potential application in wireless communication systems. At 850 MHz, a power added efficiency of 72 % and an output power of 31.5 dBm was achieved at V_{ds}=3.0V. An optimized HFET achieved 73% PAE at an output power of 30 dBm at V_{ds}=2.0V. The device exhibited an out-of-band noise performance of -112 dBm/30kHz bandwidth, a 12 dB improvement over an ion implanted MESFET.

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